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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/992,637	11/06/2001	Govind Kizhepat	GKIZ 1000-1	5830

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EXAMINER	
STEVENS, ROBERT	

ART UNIT	PAPER NUMBER
2176	

DATE MAILED: 04/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/992,637	KIZHEPAT, GOVIND	
	Examiner	Art Unit	
	Robert M Stevens	2176	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to communications: **Application No. 09/992,637** amendment filed 12/2/2004 to the original application filed 11/6/2001 by Kizephat entitled "Method and Apparatus for Performing Computations and Operations on Data Using Data Steering".

2. The Office withdraws objections raised in the First Action on the Merits (FAOM) concerning the Abstract, in light of the amendment.

3. The Office withdraws claims rejections under 35 USC 101 raised in the FAOM, in light of the amendment.

4. The Office withdraws claims rejections under 35 USC 112 2nd paragraph raised in the FAOM, in light of the amendment.

5. The FAOM rejections of claims 1, 2, 4, 5, 9-13, 15, 16, 20-23 and 25-32 under 35 USC 103(a) as being unpatentable over Derfler in view of Comer, have been withdrawn as necessitated by amendment.

6. The FAOM rejections of claims 6-8, 17-19, 24 and 33 under 35 USC 103(a) as being unpatentable over Derfler in view of Comer and Stevens, have been withdrawn as necessitated by amendment.

7. The FAOM rejections of claims 3 and 14 under 35 USC 103(a) as being unpatentable over Derfler in view of Comer and Antonov, have been withdrawn as necessitated by amendment.

8. Claims 1-33 are pending. Claims 1, 12, 23 and 29 are independent.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. **Claims 1-33 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Athanas et al. (US Patent No. 5,828,858, filed Sep. 16, 1996 and issued Oct. 27, 1998, hereafter referred to as "Athanas") in view of Hillis et al. (US Patent No. US 5,590,283, filed Jan. 27, 1995 and issued Dec. 31, 1996, hereafter referred to as "Hillis").

Regarding independent method claim 1, Athanas discloses:

> *A data processing system, comprising:*
> *a plurality of functional units having respective inputs and outputs, and adapted to perform respective tasks using input data at the respective inputs and to supply output data at the respective outputs, ... ;* (Fig. 4)
> *a plurality of routing units, responsive to respective routing control signals and coupled to the plurality of functional units, by which data is steered among the plurality of functional units;* (Fig. 3 #32 Crossbar Network and col. 4 lines 33-36) *and*

control word distribution circuitry which supplies control words the routing control signals in parallel to the plurality of routing units to establish a route ... . (Fig. 2 #21)

Athanas, however, does not explicitly disclose:

... :

... , within a function cycle;
... ; and
... for a function cycle control words.

Hillis, though, discloses:

... :

... , within a function cycle; (col. 6 lines 36-38 discuss the well known concept of synchronous processing)
... ; and
... for a function cycle control words. (col. 6 lines 36-38 discuss the well known concept of synchronous processing)

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Hillis for the benefit of Athanas, because to do so would have allowed a computing system implementer to control large numbers of processors while facilitating data flows, as taught by Hillis in col. 1 lines 25-29. These references were all applicable to the same field of endeavor, i.e., computer architecture.

Regarding claim 2, which is dependent upon claim 1, Athanas discloses:

wherein said plurality of routing units includes at least one multiplexer having a plurality of inputs and coupled to respective functional units in the plurality of functional units (Fig. 3 #32, #33) *and at least one output coupled to a functional unit in the plurality of functional units* (Fig. 3 #32, #33), *and the routing control signal for the multiplexer specifies one of a plurality of inputs to indicate a source functional unit, and one of the at least one outputs to indicate a destination functional unit.* (Fig. 2 #21)

Regarding claim 3, which is dependent upon claim 1, Athanas discloses:

> *wherein said plurality of routing units includes at least one crossbar switch.* (Fig. 3 #32)

Regarding claim 4, which is dependent upon claim 1, Athanas discloses:

> *wherein said plurality of functional units includes at least one storage element.* (col. 8 lines 12-16, esp. "registers")

Regarding claim 5, which is dependent upon claim 1, the limitations of claim 1 have been previously discussed.

Athanas, however, does not explicitly disclose:

> *wherein said plurality of functional units includes at least one logic block which performs a plurality of available functions, and includes logic to select an output from one of the plurality of available functions in response to a routing control signal in the control.*

Hillis, though, discloses:

> *wherein said plurality of functional units includes at least one logic block which performs a plurality of available functions, and includes logic to select an output from one of the plurality of available functions in response to a routing control signal in the control.* (Fig. 1 #11(0) - #11(N), noting interfaces to control network and data router)

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Hillis for the benefit of Athanas, because to do so would have allowed a computing system implementer to control large numbers of processors while facilitating data

flows, as taught by Hillis in col. 1 lines 25-29. These references were all applicable to the same field of endeavor, i.e., computer architecture.

Regarding claim 6, which is dependent upon claim 1, Athanas discloses:

> *wherein said plurality of functional units includes a memory responsive to addresses, write control signals, and read control signals, and the control word distribution circuitry supplies at least one of the write control signals and read control signals.* (Fig. 2 #21 shows control words and col. 5 lines 51-56 discuss read and write operations)

Regarding claim 7, which is dependent upon claim 6, the limitations of claim 6 have been previously discussed.

Athanas, however, does not explicitly disclose:

> *wherein said control word the control word distribution circuitry supplies an address for said memory.*

Hillis, though, discloses:

> *wherein said control word the control word distribution circuitry supplies an address for said memory.* (Fig. 1 #15, it being merely a matter of obvious design choice as to what hardware component provides what information [e.g., an address])

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Hillis for the benefit of Athanas, because to do so would have allowed a computing system implementer to control large numbers of processors while facilitating data

flows, as taught by Hillis in col. 1 lines 25-29. These references were all applicable to the same field of endeavor, i.e., computer architecture.

Regarding claim 8, which is dependent upon claim 6, the limitations of claim 6 have been previously discussed.

Athanas, however, does not explicitly disclose:

> *wherein an address for said memory is supplied by one of the plurality of functional units.*

Hillis, though, discloses:

> *wherein an address for said memory is supplied by one of the plurality of functional units.* (Fig. 1 #11(0) - #11(N), it being merely a matter of obvious design choice as to what hardware component provides what information [e.g., an address])

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Hillis for the benefit of Athanas, because to do so would have allowed a computing system implementer to control large numbers of processors while facilitating data flows, as taught by Hillis in col. 1 lines 25-29. These references were all applicable to the same field of endeavor, i.e., computer architecture.

Regarding claim 9, which is dependent upon claim 1, Athanas discloses:

> *wherein functional units in the plurality of functional units comprise logic dedicated to specific processing tasks* (col. 6 lines 12-16)

Regarding claim 10, which is dependent upon claim 1, Athanas discloses:

wherein functional units in the plurality of functional units comprise hardwired logic dedicated to specific processing tasks. (col. 5 lines 57-64, it being merely a matter of obvious design choice whether to tie together a particular set of hardware components [and which such components])

Regarding claim 11, which is dependent upon claim 1, the limitations of claim 1 have been previously discussed.

Athanas, however, does not explicitly disclose:

wherein said control word logic distribution circuitry supplies said control routing control signals synchronously to the plurality of functional units.

Hillis, though, discloses:

wherein said control word logic distribution circuitry supplies said control routing control signals synchronously to the plurality of functional units. (Fig. 1 #15. and col. 6 lines 36-38 discussing the well known concept of synchronous processing)

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Hillis for the benefit of Athanas, because to do so would have allowed a computing system implementer to control large numbers of processors while facilitating data flows, as taught by Hillis in col. 1 lines 25-29. These references were all applicable to the same field of endeavor, i.e., computer architecture.

Regarding independent method claim 12, Athanas discloses:

A data processing system, comprising:
... ;
... ; and
... ;

wherein processing blocks in said plurality of processing blocks respectively include:

a plurality of functional units having respective inputs and outputs, and adapted to perform respective processes using input data at the respective inputs and to supply output data at the respective outputs, (Fig. 4) *... ;*

a plurality of unit level routing units, coupled to the plurality of functional units and responsive to respective routing control signals for the plurality of unit level routing units, by which data is steered among the inputs and outputs of the plurality of functional units; (Fig. 3 #2 Crossbar Network and col. 4 lines 33-36) *and*

... .

Athanas, however, does not explicitly disclose:

... :

a plurality of processing blocks having respective inputs and outputs, and adapted to perform respective processes using input data at the respective inputs and to supply output data at the respective outputs, within a function cycle;

a plurality of routing units, coupled to the plurality of processing blocks and responsive to respective routing control signals for the plurality of processing blocks, by which data is steered among the inputs and outputs of the plurality of processing blocks; and

block level control word distribution circuitry which supplies control words for respective function cycles to the plurality of routing units, said control words including the routing control signals for the plurality of routing units;

wherein processing blocks in said plurality of processing blocks respectively include:

... , within a block function cycle;

... ; and

functional unit level control word distribution circuitry which supplies control words for respective block function cycles to the plurality of unit level routing units, said control words including the routing control signals for the plurality of unit level routing units.

Hillis, though, discloses:

... :

a plurality of processing blocks having respective inputs and outputs, and adapted to perform respective processes using input data at the respective inputs and to supply output data at the respective outputs, within a function cycle; (Fig. 1 #11(0) - #11(N))

> *a plurality of routing units, coupled to the plurality of processing blocks and responsive to respective routing control signals for the plurality of processing blocks, by which data is steered among the inputs and outputs of the plurality of processing blocks;* (Fig. 1 #14) *and*
>
> *block level control word distribution circuitry which supplies control words for respective function cycles to the plurality of routing units, said control words including the routing control signals for the plurality of routing units;* (Fig. 1 #15, #14)
>
> *wherein processing blocks in said plurality of processing blocks respectively include:*
>
> *... , within a block function cycle;* (col. 6 lines 36-38)
>
> *... ; and*
>
> *functional unit level control word distribution circuitry which supplies control words for respective block function cycles to the plurality of unit level routing units, said control words including the routing control signals for the plurality of unit level routing units.* (Fig. 1 #15 and col. 6 lines 36-38)

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Hillis for the benefit of Athanas, because to do so would have allowed a computing system implementer to control large numbers of processors while facilitating data flows, as taught by Hillis in col. 1 lines 25-29. These references were all applicable to the same field of endeavor, i.e., computer architecture.

Claims 13-21 are substantially similar to claims 2-10, respectively, and therefore likewise rejected.

Regarding claim 22, which is dependent upon claim 12, the limitations of claim 12 have been previously discussed.

Athanas, however, does not explicitly disclose:

wherein at least one of said block level control word distribution circuitry and functional level control word logic supplies distribution circuitry supplies said control words synchronously.

Hillis, though, discloses:

wherein at least one of said block level control word distribution circuitry and functional level control word logic supplies distribution circuitry supplies said control words synchronously. (Fig. 1 #15 and col. 6 lines 36-38)

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Hillis for the benefit of Athanas, because to do so would have allowed a computing system implementer to control large numbers of processors while facilitating data flows, as taught by Hillis in col. 1 lines 25-29. These references were all applicable to the same field of endeavor, i.e., computer architecture.

Regarding independent method claim 23, Athanas discloses:

A method of processing data, in a data processing engine that includes a plurality of functional units (Fig. 4), *comprising:*

... among the plurality of functional units; (Fig. 4) *and*

... and performing tasks in the plurality of functional units using the route to produce a result. (col. 6 lines 12-24)

Athanas, however, does not explicitly disclose:

... :

providing a set of software routing control signals in parallel to a set of routing units in the data processing engine to specify a route ... ; and

routing data among the plurality of functional units according to the set of software words routing control signals ... .

Hillis, though, discloses:

... :

> *providing a set of software routing control signals in parallel to a set of routing units in the data processing engine to specify a route* (Fig. 1 #15) ... ; *and*
> *routing data among the plurality of functional units according to the set of software words routing control signals* ... . (Fig. 1 #15)

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Hillis for the benefit of Athanas, because to do so would have allowed a computing system implementer to control large numbers of processors while facilitating data flows, as taught by Hillis in col. 1 lines 25-29. These references were all applicable to the same field of endeavor, i.e., computer architecture.

Regarding claim 24, which is dependent upon claim 23, Athanas discloses:

> *compiling a high level programming language specifying the result to produce the set of software words routing control signals.* (Fig. 7 and col. 10 line 59 – col. 11 line 10, esp. "compile time" and "library")

Claims 25-26 are substantially similar to claims 9-10, respectively, and therefore likewise rejected.

Regarding claim 27, which is dependent upon claim 23, the limitations of claim 23 have been previously discussed.

Athanas further discloses:

> ... , *and said set of routing control signals specify data paths through the plurality of switches.* (Abstract, esp. pathways discussion)

Athanas, however, does not explicitly disclose:

> *wherein the routing units in the data processing engine comprise a plurality of switches interconnecting the plurality of functional units, ...*

Hillis, though, discloses:

> *wherein the routing units in the data processing engine comprise a plurality of switches interconnecting the plurality of functional units, ...* (Fig. 1 #11, 14 and 15)

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Hillis for the benefit of Athanas, because to do so would have allowed a computing system implementer to control large numbers of processors while facilitating data flows, as taught by Hillis in col. 1 lines 25-29. These references were all applicable to the same field of endeavor, i.e., computer architecture.

Regarding claim 28, which is dependent upon claim 23, the limitations of claim 23 have been previously discussed.

Athanas, however, does not explicitly disclose:

> *including synchronously routing said data among the plurality of functional units.*

Hillis, though, discloses:

> *including synchronously routing said data among the plurality of functional units.* (Fig. 1 #15, and col. 6 lines 36-38 discusses the well known concept of synchronous processing)

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Hillis for the benefit of Athanas, because to do so would have allowed a

computing system implementer to control large numbers of processors while facilitating data flows, as taught by Hillis in col. 1 lines 25-29. These references were all applicable to the same field of endeavor, i.e., computer architecture.

Regarding independent method claim 29, Athanas discloses:

> *A method of processing data, in a data processing engine that includes a plurality of functional units* (Fig. 4),*comprising:*
>
> *... ;*
>
> *performing tasks in said plurality of first functional units using the first data path;* (Fig. 4 and col. 8 lines 12-24 and Abstract discussions)
>
> *... ; and*
>
> *performing tasks in said plurality of functional units using the second data path to accomplish said different function.* (Fig. 4 and col. 8 lines 12-24 and Abstract discussions)

Athanas, however, does not explicitly disclose:

> *... :*
>
> *providing a first set of software routing control signals in parallel to said set of routing units to specify a first data path according to a first configuration of the plurality of functional units;*
>
> *... ;*
>
> *providing a second set of software routing control signals that in parallel to said set of routing units to specify a second data path according to a second configuration of the plurality of functional units, whereby the plurality of functional units is reconfigured to perform a different function; and*
>
> *... .*

Hillis, though, discloses:

> *... :*
>
> *providing a first set of software routing control signals in parallel to said set of routing units to specify a first data path according to a first configuration of the plurality of functional units;* (Fig. 1 #11, 14 and 15 and interconnecting paths)
>
> *... ;*
>
> *providing a second set of software routing control signals that in parallel to said set of routing units to specify a second data path according to a second configuration of the plurality of functional units, whereby the plurality of*

functional units is reconfigured to perform a different function; (Fig. 1 #11, 14 and 15 and interconnecting paths) *and*

... .

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Hillis for the benefit of Athanas, because to do so would have allowed a computing system implementer to control large numbers of processors while facilitating data flows, as taught by Hillis in col. 1 lines 25-29. These references were all applicable to the same field of endeavor, i.e., computer architecture.

Claims 30-31 are substantially similar to claims 9-10, respectively, and therefore likewise rejected.

Claims 32-33 are substantially similar to claims 27 and 24, respectively, and therefore likewise rejected.

Response to Arguments

11. Applicant's arguments filed 12/16/2004 have been fully considered but they are not persuasive.

Applicant's remarks on page 12 of the amendment concerning the "Objection to the Abstract", "Rejection of Claims Under 35 USC 101", "Rejection of Claims Under 35 USC 112, 2nd paragraph" raised in the FAOM have been addressed above.

It is respectfully noted that Applicant's amendment to the claims significantly changes the scope of the claimed invention as a whole. As such, Applicant's arguments (pages 11-15 of

the amendment) concerning FAOM rejections of claims 1-33 under 35 USC 103(a) have been rendered moot.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

	US Patents
Bartowiak et al	5,771,362
Sonnier et al	5,751,955
Chan et al	5,726,930
Halverson, Jr., et al	5,574,930
Grondalski	5,481,749
Baxter	5,481,743
Gifford	5,418,970
Peters et al	4,445,172

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert M Stevens whose telephone number is (571) 272-4102. The examiner can normally be reached on M-F 6:00 - 2:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Joseph H. Feild can be reached on (571) 272-4090. The current fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Additionally, the main number for Technology Center 2100 is (571) 272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Robert M. Stevens
Reg. No. 47,972
Art Unit 2176
Date: April 16, 2005

JOSEPH FEILD
SUPERVISORY PATENT EXAMINER

rms